



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/765,311

01/26/2004

Dennis Wendell

SUNMP383

9410

32291

7590

03/01/2005

MARTINE PENILLA & GENCARELLA, LLP  
710 LAKEWAY DRIVE  
SUITE 200  
SUNNYVALE, CA 94085

EXAMINER

NGUYEN, HIEP

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

<b>Office Action Summary</b>	<b>Application No.</b> 10/765,311	<b>Applicant(s)</b> WENDELL ET AL.	
	<b>Examiner</b> Hiep Nguyen	<b>Art Unit</b> 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 01-26-04.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Specification*

The disclosure is objected to because of the following informalities: the disclosure “the pull down logic 221” in section [0028], page 13 is misleading because circuit (221) is a latch. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and / or clarification is required.

Regarding claim 1, the recitation “the sense stage being configured to receive and amplify a higher signal to be provided by the pair of balance isolation devices of the input stage” is indefinite because it is not clear what “a higher signal” is meant by and how the “pair of balance isolation devices” can provide “a higher signal”.

Regarding claims 9, 19, 20 and 29, the recitation “pull down logic” in claims 9, 19 and “pull down circuitry” in claims 20 and 29 are indefinite because they are misdescriptive. Element (221) in figure 2B of the present application is only a latch. The voltage at the input/output of the latch can be high or low depending on the outputs of the balanced isolation device (223). Circuit (221) is not a “pull down logic” as recited.

Regarding claim 14, the recitation “a pair of charging devices each being configured to supply a steady voltage to a separate one of the pair of input nodes” is indefinite because it is misdescriptive. The charging device (213) will not supply a voltage to the input nodes when it is not enabled i.e., voltage (rec\_sig) is high.

Regarding claim 26, the recitation “connecting an output of each of a second pair of PMOS devices to a separate one of the pair of input nodes” is indefinite because it is not clear what is the “a second pair of PMOS devices” in the drawing. Assume that the “second pair

Art Unit: 2816

of PMOS devices” comprises transistors (M8) and (M9) then the **first** pair of PMOS is not seen in the drawing.

Claims 2-8, 10-13, 15-18, 21-25, 27 and 18 are indefinite because of the technical deficiencies of claim 1, 9 and 20.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-16, 19-24 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure (US Pat. 5,455,802).

Regarding claims 1-4, figure 2 of McClure shows a sense amplifier comprising:

an input stage having a pair of balanced isolation devices, each of the pair of balanced isolation devices (34, 36) having an input connected to receive a separate one of a pair of differential input signals (I/O, I/O/), each of the pair of balanced isolation devices having a gate connected to receive a common bias voltage (ISO); and

a sense stage (28, 30, 32, 38, 40) connected to the input stage, the sense stage being configured to receive and “amplify a higher signal” to be provided by the pair of balanced isolation devices of the input stage. Note that the output signals from the input stage is “amplified” by the “recovering stage” (28, 32). The balanced isolation devices (34, 36) are PMOS. It is inherent that the common bias voltage is (ISO) is generated by a bias generator circuit.

Regarding claims 6 and 7, the sense nodes are nodes (42) and (44). The transmission gate (30) is controlled by the equalization control signal (EQ) and acts as an equalization device.

Regarding claim 8, the booster circuit (28, 32) is also control by the equalization control signal (EQ).

Regarding claims 9-11, figure 2 of McClure shows a sense amplifier, comprising

Art Unit: 2816

a pair of input nodes connected to each receive a separate one of a pair of differential input signals (I/O, I/O/);

a pair of balanced isolation devices are PMOS (34) and PMOS (36) each having an input connected to a separate one of the pair of input nodes, the pair of balanced isolation devices each having a gate connected to receive a common bias voltage (ISO), the pair of balanced isolation devices each having an output representing a separate one of a pair of sense nodes (42, 44);

a transmission gate (30) disposed between the pair of sense nodes, the transmission gate being configured to control conduction between the pair of sense nodes; and

“pull down logic” (38, 40) being connected to the pair of sense nodes.

Transmission gate (30) having terminals coupled to the sense nodes (42) and (44).

Regarding claims 12 and 16, the booster devices (28) and (32) boost the voltage of the sense nodes. It is inherent that the common bias voltage is (ISO) is generated by a bias generator circuit.

Regarding claim 19, the “pull down logic” comprises NMOS transistors (38, 40).

Regarding claims 20-23, figure 2 of McClure shows a method for making a sense amplifier, comprising:

connecting a pair of input nodes to each receive a separate one of a pair of differential input signals (I/O, I/O/);

connecting an input of each of a pair of balanced isolation devices (34, 36) to a separate one of the pair of input nodes, wherein each of the pair of balanced isolation devices has an output representing a separate one of a pair of sense nodes (42, 44);

connecting a gate of each of the pair of balanced isolation devices to receive a common bias voltage (ISO);

connecting each of a first terminal and a second terminal of a transmission gate (30) to a separate one of the pair of sense nodes; and

connecting “pull down circuitry” (38, 40) to the pair of sense nodes (42, 44).

The balanced isolation devices comprise PMOS (34) and (36) and the transmission gate comprises PMOS (30). The gate of transmission gate (30) receives an equalization control signal (EQ).

Art Unit: 2816

Regarding claim 24, the booster devices (28) and (32) boost the voltage of the sense nodes (42) and (44) when activated.

Regarding claim 29, the "pull down logic" comprises NMOS transistors (38, 40).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure (US Pat. 5,455,802).

Regarding claims 5, 17 and 17, figure 2 of McClure includes all the limitations of these claims except for the limitation that the common bias voltage is maintained at a level about one-half of a supply voltage level. However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d

Art Unit: 2816

1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the common bias voltage at a level about one-half of a supply voltage level dependent upon particular environment of use to ensure optimum performance. Note that the PMOS transistors (T3) and (T4) need a voltage slightly higher than the threshold of the PMOS transistors to turn them off.

### ***Allowable Subject Matter***

Claims 13, 14, 18, 25, 26 and 28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claims 13, 14, 18, 25, 26 and 28 would be allowable because the prior art of record (UA Pat. 5,455,802) fails to teach or suggest a pair of booster devices comprising NAND gates as called for in claims 13 and 25; a pair of charging devices or a recovery stage comprising PMOS transistors for charging the pair of input nodes as called for in claims 14, 18, 26 and 28.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

02-25-05



TUAN T. LAM  
PRIMARY EXAMINER